forming a semiconductor extension to the top one of the semiconductor layers such that a portion of the grown semiconductor is located between the extension and the substrate.

8. An integrated circuit, comprising:

a substrate having a planar surface;

collector, base, and emitter semiconductor layers of a bipolar transistor, the semiconductor layers forming a vertical sequence on the substrate in which intrinsic portions of two of the layers are sandwiched between the substrate and a remaining top one of the layers; and

wherein the base layer comprises an extrinsic semiconductor extension that laterally encircles a vertical portion of the top one of said semiconductor layers.

9. The apparatus of claim 8, further comprising:

a dielectric sidewall interposed between the vertical portion of the top one of the layers and the extension of the base layer.

10 ~~11~~. The apparatus of claim 8, wherein the extension of the base layer extends farther away from the substrate than an interface between the top one of the semiconductor layers and the base layer.

11 ~~12~~. The apparatus of claim 8, wherein one of the two of the semiconductor layers is a doped region of the substrate.

12 ~~13~~. The apparatus of claim 8, further comprising:

a semiconductor extension to the top one of the layers, part of the extension of the base layer being located between the substrate and the extension of the top one of the layers.

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